REMARKS

Applicant appreciates the time taken by the Examiner to review Applicant's present application. This application has been carefully reviewed in light of the Official Action mailed December 27, 2004. Claim 21 has been amended. Claims 1-31 remain pending in the case. Applicant respectfully requests reconsideration and favorable action in this case.

Rejections under 35 U.S.C. § 102

Claims 1, 7, 9 and 11-12 stand rejected as anticipated by U.S. Patent No. 6,434,115 ("Schwartz"). The standard for "anticipation" is one of fairly strict identity. A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference. *Verdegaal Bros. V. Union Oil Co. of California*, 814 F.2d 628, 631, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987), MPEP § 2131. Furthermore, anticipation requires the presence in a single prior art reference disclosure of each and every element of the claimed invention, arranged as in the claim. *W.L. Gore & Assocs. v. Garlock*, 721 F.2d 1540, 220 USPQ 303 (Fed. Cir. 1983).

Claim 1 recites:

> A system for transporting data from a plurality of ingress lines to a plurality of egress lines comprising:
>
> a data switching matrix having a plurality of ingress ports and a plurality of egress ports, wherein for each of the ingress ports, the data switching matrix is configured to transport data from each the ingress port to one of the plurality of egress ports
> a plurality of ingress edge units, each of which is coupled to one of the plurality of ingress ports of the data switching matrix, wherein each of the plurality of ingress edge units is configured to receive a data from a corresponding one or more of a plurality of ingress lines
> a plurality of egress edge units, each of which is coupled to one of the plurality of egress ports of the data switching matrix, wherein each of the plurality of egress edge units is configured to transmit data received from the data switching matrix to one or more of a plurality of egress lines
> wherein each of the plurality of ingress edge units is configured to examine data received via the corresponding ingress lines and to identify portions of the data corresponding to each of the egress edge units, wherein portions of the data corresponding to each of the egress edge units is stored in a corresponding buffer and

wherein data in each buffer is transmitted to the corresponding egress edge unit via the data switching matrix in a predetermined time slot

Thus, Claim 1 recites a system for transporting data from ingress lines to egress lines. The system includes a data switching matrix that transports data from ingress ports to egress ports, where each ingress port has an ingress edge unit and each egress port has an egress edge unit. Each ingress edge unit examines received data and identifies portions of the data corresponding to each individual egress edge unit. Portions of data corresponding to an egress edge unit are stored in that egress edge unit's corresponding buffer. In a predetermined time slot, each buffer transmits data to its corresponding egress edge unit.

Claim 11 recites:

An ingress edge unit configured to be coupled to a data switching matrix, wherein the ingress edge unit comprises:

one or more ingress ports, each of which is configured to be coupled to an ingress data line;
a switch coupled to the one or more ingress ports; and
a plurality of buffers coupled to the switch;
wherein the switch is configured to store data received via the one or more ingress ports in the plurality of buffers, wherein the data stored in each of the plurality of buffers is destined for a corresponding one of a plurality of destinations; and
wherein the ingress edge unit is configured to transmit data from each of the plurality of buffers in a corresponding predetermined time slot and wherein the ingress edge unit is configured to schedule data from each of the plurality of buffers to be delivered to the corresponding one of the plurality of destinations, independent of the predetermined time slot.

Thus, Claim 11 recites an ingress edge unit. The ingress edge unit includes a switch that can store data in buffers. Data for a particular destination is stored in the buffer corresponding to that particular destination. The ingress edge unit can transmit data from each of the buffers in a corresponding predetermined time slot. And, the ingress edge unit can schedule data from each of the buffers to be delivered to its corresponding destination independent of the predetermined time slot.

The ingress edge units of Claim 1 identify portions of data corresponding to each of the egress edge units and store portions of data corresponding to an egress edge unit in a buffer corresponding to the egress edge unit. Similarly, data input to the ingress edge unit of Claim 11 is stored by destination in respective buffers. Thus, the claimed buffers each have a corresponding destination. The input port modules of Schwartz differ from the claimed ingress edge units. Swartz recites, '[f]or each packet received, the input port module [#] buffers the packet' (Schwartz – col. 5, lines 21-22). While the input port modules of Schwartz buffer data, the input port modules of Schwartz each appear to buffer packets intended for multiple destinations at a given time. Unlike the input port modules of Schwartz, the claimed buffers each buffer data for a particular egress edge unit at a given time.

The manner in which data is transmitted from the ingress edge units to the egress edge units also differs. The ingress edge units of the pending claims either transmit data during a predetermined time slot, as recited in Claims 1 and 11, or during a time independent of a predetermined time slot and scheduled by an ingress edge unit as recited in Claim 11. The input modules of Schwartz, on the other hand, appear to send packets when the output modules request packets. As recited by Schwartz, "[f]or each meta-data packet retrieved by an output port module, the output port module will request that the input port module identified in the meta-data packet transfer the packet identified in the input port module thereto through the packet switch" (Schwartz – Abstract). Thus, it appears the input modules of Schwartz send data when called for by the output module not in a predetermined time slot or according to a schedule.

In contrast to the claimed limitations, Schwartz teaches a system which buffers packets in input port modules without regard to packet destination. In further contrast, Schwartz teaches a system that transfers packets when packet requests are generated by the output port modules, not in predetermined time slots. Applicant submits that while the Examiner points to lines 5-8, 48-50, 12-17, 15-20, 18-21, 24-29, 21-31, and 32-35 of column 5 and lines 30-35 of column 10 of Schwartz as showing the claimed limitations, examination of these passages fails

to illustrate the claimed limitations and, therefore, Schwartz cannot be properly construed as anticipating or rendering obvious the pending claims.

Schwartz provides neither teaching nor suggestion for the system of Claim 1, which includes ingress edge units configured to examine data and identify portions of the data corresponding to each of the egress edge units, where respective portions of data are stored in each egress edge unit's corresponding buffer, and where data in each buffer is transmitted to its corresponding egress edge unit in a predetermined time slot. Similarly, Schwartz provides neither teaching nor suggestion for the ingress edge unit of Claim 11, which includes a switch that can store data in buffers, where data for a particular destination is stored in the buffer corresponding to the particular destination, and where an ingress edge unit can transmit data from each of the buffers in a corresponding predetermined time slot, as well as schedule data from each of the buffers to be delivered to its corresponding destination independent of the predetermined time slot. Therefore, Schwartz does not and cannot anticipate the limitations of independent Claims 1 and 11. Further, Schwartz provides no suggestion or motivation to modify such that the limitations of independent Claims 1 and 11 are met. Consequently, the cited art does not render the claimed limitations obvious, and independent Claims 1 and 11 are patentably distinct in view of the cited art. Claims 7 and 9 are dependent from Claim 1 and claim 12 is dependent from Claim 11. Thus, Claims 7, 9, and 12 are also patentably distinct. For at least these reasons, withdrawal of this rejection is respectfully requested

Claims 20-21 and 25 stand rejected as anticipated by U.S. Patent No. 5,126,999 ("Munter"). The standard for "anticipation" is one of fairly strict identity. A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference. *Verdegaal Bros. V. Union Oil Co. of California*, 814 F.2d 628, 631, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987), MPEP § 2131. Furthermore, anticipation requires the presence in a single prior art reference disclosure of each and every element of the claimed invention, arranged as in the claim. *W.L. Gore & Assocs. v. Garlock*, 721 F.2d 1540, 220 USPQ 303 (Fed. Cir. 1983).

Claim 20 recites:

A method comprising:

examining pieces of data in a received data stream;
identifying a destination for each piece of data;
storing the pieces of data in a plurality of buffer units, wherein for each buffer unit, all of the pieces of data stored therein have a common destination; and
transmitting data from each buffer unit in a corresponding periodic timeslot.

Thus, Claim 20 of recites a method including examining data, identifying data destination, and storing data in a buffer unit according to data destination such that all data in the buffer unit has a common destination. Further, the claimed method includes transmitting data from each buffer unit in a corresponding periodic timeslot.

Claim 21 has been amended to recite:

A method for transporting data comprising:

parsing a received data stream into a plurality of data cells;
identifying a destination corresponding to each of the plurality of data cells;
segregating the plurality of data cells into distinct sets of data cells, wherein the data cells in each set of data cells has a common destination; and
sequentially transmitting the sets of data cells to their respective ~~corresponding~~ destinations, wherein each set of data is transmitted to each destination in a timeslot corresponding to that destination.

Thus, Claim 21 recites a method including parsing data into data cells, identifying each data cell's destination, and segregating data cells having common destinations together in data sets. Further, the claimed method includes sequentially transmitting the data sets to their respective destinations during a timeslot which corresponds to the destination.

Munter discloses a method and apparatus for input-buffered asynchronous transfer mode switching. However, Munter does not disclose each and every element set forth in the pending claims, some distinctions of which are set forth below.

Claims 20 and 21 include methods of transmitting buffered common-destination data in a corresponding periodic timeslot and transmitting common-destination data sequentially. Thus, in Claim 20, data is sent out from a buffer in a periodic timeslot and in Claim 21 the data is sent out from each buffer in a time slot corresponding to a destination according to a sequence. In contrast to the claimed limitations, Munter teaches a switching matrix having 'N' input ports. Each input port is buffered by an output-segregated input buffer, and each output-segregated input buffer includes 'N' independent FIFO buffers which store data packets having the same output port destination (Munter, col. 5, lines 28-33). Status of input packets and buffers is reflected dynamically upon an input buffer map. The input buffer map is operated on by an 'N' crosspoint selector to yield a new selection of 'N' crosspoints for each packet cycle on a realtime basis. (Munter, col. 5, lines 30-48). Thus, it appears the FIFO buffer from which data is sent in a given cycle is arbitrarily determined based on the dynamic load at the switching matrix. Data is not sent from each FIFO in a "periodic timeslot" or in a "time slot corresponding to a destination" based on a particular sequence.

Munter provides neither teaching nor suggestion for the claimed limitations. Although Munter appears to teach a method of buffering data according to destination and transferring data periodically, Munter teaches selecting 'N' crosspoints for each packet cycle where the 'N' crosspoints are selected by a crosspoint selector. Therefore, Munter cannot be construed as transmitting common-destination data in a corresponding periodic timeslot as claimed by Claim 20. Further, Munter cannot be construed as sequentially transmitting data sets to their respective destinations, where each set of data is transmitted to each destination in a timeslot corresponding to that destination as claimed by currently amended Claim 21. Consequently, Munter does not anticipate the limitations of independent Claims 20 and 21. Nor does Munter provide suggestion or motivation to modify such that the claimed limitations are met. Consequently, the cited art does not render the claimed limitations obvious, and independent

Claim 25 depends from Claim 21. Thus, Claim 25 is also patentably distinct. For at least these reasons, withdrawal of this rejection is respectfully requested

Allowable Subject Matter

Claims 2-6, 8, 10, 13-19, 22-24 and 26-31 stand currently objected to as dependent on a rejected base claim but allowable if rewritten in independent form including al of the limitations of the base claim and any intervening claims. Examiner's recognition of patentable subject matter is appreciated. In view of the above reply, Applicant believes Examiner will find the base claims to also be patentable. Accordingly, withdrawal of this objection is respectfully requested.

Applicant has now made an earnest attempt to place this case in condition for allowance. Other than as explicitly set forth above, this reply does not include an acquiescence to statements, assertions, assumptions, conclusions, or any combination thereof in the Office Action. For the foregoing reasons and for other reasons clearly apparent, Applicant respectfully requests full allowance of Claims 1, 7, 9, 11, 12, 20, 21, and 25, in addition to those claims previously adjudged allowable. The Examiner is invited to telephone the undersigned at the number listed below for prompt action in the event any issues remain.

The Director of the U.S. Patent and Trademark Office is hereby authorized to charge any fees or credit any overpayments to Deposit Account No. 50-3183 of Sprinkle IP Law Group.

Respectfully submitted,

Sprinkle IP Law Group
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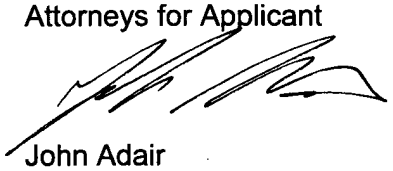

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